The data on the position and movement of the stylus is also provided to handwriting recognition software, which is stored in the ROM **221** and/or the RAM **222**. The handwriting recognizer suitably converts the written instructions from the user into text data suitable for saving time and expense information. The process of converting the pen strokes into equivalent characters and/or drawing vectors using the handwriting recognizer is described below.

[**0061**] The computer system is also connected to one or more input/output (I/O) ports **242** which allow the CPU **220** to communicate with other computers. Each of the I/O ports **242** may be a parallel port, a serial port, a universal serial bus (USB) port, a Firewire port, or alternatively a proprietary port to enable the computer system to dock with the host computer. In the event that the I/O port **242** is housed in a docking port, after docking, the I/O ports **242** and software located on a host computer (not shown) support an automatic synchronization of data between the computer system and the host computer. During operation, the synchronization software runs in the background mode on the host computer and listens for a synchronization request or command from the computer system **200** of the present invention. Changes made on the computer system and the host computer will be reflected on both systems after synchronization. Preferably, the synchronization software only synchronizes the portions of the files that have been modified to reduce the updating times. The I/O port **242** is preferably a high speed serial port such as an RS-232 port, a Universal Serial Bus, or a Fibre Channel for cost reasons, but can also be a parallel port for higher data transfer rate.

[**0062**] One or more portable computers **200** can be dispersed in nearby cell regions and communicate with a cellular mobile support station (MSS) as well as a Bluetooth station. The cellular and Bluetooth stations relay the messages via stations positioned on a global basis to ensure that the user is connected to the network, regardless of his or her reference to home. The stations are eventually connected to the Internet, which is a super-network, or a network of networks, interconnecting a number of computers together using predefined protocols to tell the computers how to locate and exchange data with one another. The primary elements of the Internet are host computers that are linked by a backbone telecommunications network and communicate using one or more protocols. The most fundamental of Internet protocols is called Transmission Control Protocol/Internet Protocol (TCP/IP), which is essentially an envelope where data resides. The TCP protocol tells computers what is in the packet, and the IP protocol tells computers where to send the packet. The IP transmits blocks of data called datagrams from sources to destinations throughout the Internet. As packets of information travel across the Internet, routers throughout the network check the addresses of data packages and determine the best route to send them to their destinations. Furthermore, packets of information are detoured around non-operative computers if necessary until the information finds its way to the proper destination.

[**0063**] Although specific embodiments of the present invention have been illustrated in the accompanying drawings and described in the foregoing detailed description, it will be understood that the invention is not limited to the particular embodiments described herein, but is capable of numerous rearrangements, modifications, and substitutions without departing from the scope of the invention. The following claims are intended to encompass all such modifications.

What is claimed is:

1. A low power a reconfigurable processor core, comprising:

one or more processing units, each unit having a clock input that controls the performance of the unit;

a wireless transceiver transmitting and receiving at a frequency based on a wireless clock input; and

a controller having a plurality of clock outputs each coupled to the clock inputs of the processing units and the wireless clock input, the clock outputs being generated from a common master clock.

2. The processor core of claim 1, wherein the common master clock operates at the same frequency as a Bluetooth frequency or an 802.11 frequency.

3. The processor core of claim 1, wherein one of the processing unit comprises a digital signal processor (DSP) or a reduced instruction set computer (RISC) processor.

4. The processor core of claim 1, wherein each unit is dynamically managed on a per-task basis.

5. The processor core of claim 1, wherein each unit is clocked at the lowest rate possible to reduce peak power dissipation, reduce average power dissipation, or minimize buffer memory size and power.

6. The processor core of claim 1, wherein the controller generates a plurality of clock signals, each independently rate controlled to each processing unit.

7. The processor core of claim 1, wherein the master clock is approximately 2.4 Gigahertz.

8. The processor core of claim 1, wherein the plurality of clocks comprise gated versions of a master clock.

9. The processor core of claim 1, wherein the controller changes the clock rate of each processing unit independently of the remaining processing unit.

10. The processor core of claim 9, wherein the clock rate is generated based on an algorithm.

11. The processor core of claim 10, wherein the algorithm is optimized for one of the following: power reduction, buffer memory management, or emissions control.

12. The processor core of claim 11, wherein the algorithm is pre-assigned based upon tasks or routines handled by each processing unit.

13. The processor core of claim 11, wherein the algorithm is invoked by one or more external or internal system stimuli.

14. The processor core of claim 1, wherein the controller changes on or more clock inputs on-the-fly.

15. The processor core of claim 1, wherein the controller controls one or more clock inputs in a centralized manner.

16. The processor core of claim 1, wherein the controller controls one or more clock inputs in a decentralized manner.

17. The processor core of claim 1, wherein the controller controls one or more clock inputs in a centralized manner.

18. The processor core of claim 1, further comprising one or more clock traces coupled to the controller.

19. The processor core of claim 18, wherein each clock trace comprises an antenna.

20. The processor core of claim 18, wherein each clock trace receives power from an external power source.

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